[Low Voltage Programmable eFuse with Differential Sensing Scheme]

DESCRIPTION

Background of Invention

[Para 1] Field of the Invention

[Para 2] The present invention relates to the application of electronically programmable fuses (eFuse) in integrated circuits. An electronically programmable fuse is disclosed with a low voltage programming capability and differential sensing scheme.

[Para 3] Background of Invention

[Para 4] With continued scaling in semiconductor technologies to increasingly smaller geometries, on-chip eFuse implementations provide an attractive alternative to conventional fusing schemes for integrated circuits. In terms of area efficiency and performance impact eFuse technology presents a significant improvement over fuse technologies with optical based programming.

[Para 5] Programmable devices for integrated circuits require a dependable methodology for customizing a device in a repeatable and reliable manner. Fusing of programmable connections in microprocessors, FPGAs and other VLSI designs is a common technique to achieve the flexibility of programmability.

[Para 6] The eFuse device fabricated in silicon based integrated circuits is typically programmed using a large voltage, relative to the operating voltage of the integrated circuit, to melt and separate the fuse body material. This process changes the fuse material from a low resistance to a high resistance,

which may be measured by "sensing" circuitry to determine whether or not the eFuse has been programmed.

[Para 7] As process technology for integrated circuits has progressed, maximum operating voltages have scaled commensurately downward with physical geometry, making it difficult to provide sufficient voltage to program the eFuse without damaging logic circuitry associated with the fuse bank. In addition, the current density requirements for metal interconnect layers used to supply eFuse programming currents are typically much greater than for signal interconnect lines. As such, fuse programming buses must be implemented with wide metal wires that consume a disproportionate amount of interconnect resources. Furthermore, eFuse devices may require multiple programming pulses to ensure adequate resistance levels for the eFuse device, thereby increasing programming and test time cycles. However, repeated programming may also lead to an unfused condition in the programmed fuse if a sufficiently high voltage is applied. In that instance, the heating associated with re-programming may cause the fuse material to rejoin thereby further degrading fuse related yield.

[Para 8] Common applications for e-Fuse technology include memory array redundancy, package identification coding and post-manufacture programming of logical functions. Since each eFuse is a single primitive device, additional logic and circuitry are necessary to facilitate programming and sensing.

[Para 9] The eFuse programming operation involves sending a large current through the fuse (e.g., 15mA) for a sufficient time to dramatically change the fuse resistance from an unprogrammed resistance of about 150 Ωto a resistance of about 50 KΩ. Existing schemes require a high voltage (e.g., 3.3V) to achieve adequate fuse programming current such that all fuses are guaranteed to have a high post-programming resistance. Insufficient programming current may result in a number of fuses exhibiting much lower resistance (e.g., 1KΩ), and the "yield" following the programming step will be limited by the "tail" of the Gaussian distribution of resulting fuse resistances.

In addition, a high programming voltage requires thick-oxide transistors, which, in turn, require extra processing steps to implement. Programming the fuses with a low voltage would eliminate the need for thick-oxide transistors, however, the programming current achievable at low programming voltage limits the maximum post-programming resistance and often requires multiple programming pulses to achieve the desired post fuse programming resistance. In addition, a significant number of low post-programming resistance values can result, which significantly impacts post fuse-programming yield.

[Para 10] Further, the 3.3V supply requires a dedicated package pin and tester channel (for programming at the tester). The routing of the 3.3V signal must be wide, low-resistance metal. This 3.3V supply is on during programming, but off during sensing. Therefore the 3.3V supply must be switchable to support the fuse programming function after final packaging of the integrated circuit in a chip carrier module.

[Para 11] A "sense" circuit is required to discriminate between pre-programming and post-programming resistance, and to provide digital "0" or "1" outputs respectively. Single-ended sensing schemes are known, but they are limited to the minimum resistance they can sense. Consequently, these circuits are not viable if any fuse has a low post-programming resistance. The single-ended scheme also requires an analog current-source-control voltage to be generated and routed to each individual sense circuit. Finally, this technique exhibits very poor noise rejection properties for sensing in the field and high switching activity causes additional noise on the power supply distribution network of the integrated circuit.

[Para 12] For example, Fig. 1 depicts a prior art single-ended eFuse sense scheme. A reference circuit VrefGen 10 creates a voltage VRef to control individual sense-current transistors mPi, with one for each of many fuses Fi. The input of inverter I0 is shorted to the output, establishing a voltage Vm equal to the "trip point" of a latch that would be made of two inverters identical to I0 feeding each other; OpAmp A drives an inverting stage consisting of mPRef and RRef such that Vp has the same voltage as Vm. The

OpAmp output voltage VRef then feeds sense-current transistors mPi (one for each fuse Fi), and each fuse presents voltage Vi = Ri IRef to its own sense latch, which consists of two cross coupled inverters identical to I0 feeding each other that are not shown.

[Para 13] As future technologies continue to scale downward in feature size, a potential drawback to the prior art approach is that random manufacturing process variations may cause each transistor mPi to have a unique threshold voltage, such that the sense current will differ from fuse to fuse (VRef is a low-overdrive analog signal). Another related concern is that gate leakage from the VRef signal through the gates of individual transistors mPi will limit how many fuses can share one large VrefGen circuit.

[Para 14] Differential sense schemes are known, and they are better able to handle the tail of the resistance value distribution, however, prior differential sensing techniques employ two fuses to achieve a single programmed value, and also require one large differential amplifier per programmed value, thereby increasing the overall area requirement for fuse programming and sensing operations.

[Para 15] Accordingly, a need exists for an eFuse capable of being programmed by a single low voltage pulse, which incorporates a sensing scheme less susceptible to noise and requires fewer circuit resources then conventional designs.

Summary of Invention

[Para 16] An aspect of the invention is an eFuse implementation that is programmable with a single low voltage pulse and which includes a differential sensing function capable of discriminating low levels of resistance. A preferred embodiment disclosed herein enables fuse programming at a voltage no higher than a burn-in voltage (e.g., 1.5V) for current semiconductor manufacturing processing technologies. As such, a dedicated 3.3V pin and thick-oxide transistors to switch a high voltage programming current are not

required, thereby saving additional processing steps. With low-voltage programming, a distribution tail of low post-programming resistances is expected, however, the invention also incorporates a differential sense scheme that is able to sense low resistance values with very low circuit overhead. The differential amplifier is shared across a number of fuses; the voltage reference (for differential sensing) is shared across a large number of fuses; the individual fuse-programming transistors (required both for the low-voltage scheme claimed herein and in the prior art high-voltage implementations) are shared between the program and sense operations. In addition a large PMOS switch transistor is shared across a plurality of fuses.

Brief Description of Drawings

[Para 17] Fig. 1 illustrates a schematic of a prior art single-ended sensing scheme for eFuses.

[Para 18] Fig. 2 shows a schematic diagram of the fuse programming circuitry according to a first embodiment of the invention.

[Para 19] Fig. 3 illustrates a schematic diagram of the sense circuitry coupled to the fuse programming circuitry of Fig. 2.

[Para 20] Fig. 4 shows a schematic diagram of the present invention according to a second embodiment.

[Para 21] Fig. 5 illustrates a schematic diagram of an alternative circuit to generate a reference voltage at node Vm.

[Para 22] Fig. 6 shows a schematic diagram of a parallel combination of fuses.

[Para 23] Fig. 7A depicts a schematic of an exemplar fuse select and decode logic circuit.

[Para 24] Fig. 7B show a timing diagram corresponding to the fuse select and decode operation.

Detailed Description

[Para 25] Fig. 2 depicts the primary elements of the fuse-programming circuitry for a preferred embodiment of the present invention. A large PMOS mP pulls node F to Vdd, and a single decoded signal g[j] out of the group g[15:0] may be asserted for about 200us to turn on pull-down transistor mN[j] and draw sufficient current through fuse xF[j] to change the resistance and program the fuse. Programming is accomplished by raising Vdd to about 1.5 times its normal value. However, each fuse requires only about 200us to be programmed, so the total time for all fuses to be programmed is much less compared to the time the product is subjected to 1.5 times Vdd or greater during a device "burn-in"or other diagnostic tests, such as a dynamic voltage screen. During the programming operation, an extra fuse xF used during the sense operation is shorted out by transistor mP. Transistor mP serves the function of pulling node F all the way to Vdd to provide as much current as possible to program fuse xF[j], and also to prevent any voltage across fuse xF from altering it from its original unprogrammed state.

[Para 26] Fig. 3 combines additional elements with the fuse programming circuit shown in Fig. 2 to implement the fuse sense circuitry according to a preferred embodiment of the present invention. Most notably, a differential amplifier is added to sense the voltage difference between the outputs of two voltage dividers. The first voltage divider whose output is node "F"consists of an intact reference fuse xF and of xF[j], the one fuse selected for sensing through decoded signal g[j]. The second voltage divider known as the reference voltage divider consists of resistors R1 and R0 and gating transistor mR. R0 is comprised of two components R0a and R0b which are identical to each other and identical to R1. Use of two resistors R0a and R0b to make up a single resistance R0 reduces the variation in the reference voltage divider output voltage through cancellation of edge effects common in VLSI resistors. A concern is that the DC current through the voltage divider may change the resistance of either xF or xF[j] as a result of the sense operation. However, this scheme has several features that dramatically reduce the resistance

change due to the sense operation. First, the fuse sense operation is performed at normal Vdd, rather than 1.5 times Vdd, thereby reducing the current supplied for sensing. Second, the magnitude of the current is reduced another factor of two because xF and xF[j] are coupled in series, whereas during programming only xF[j] limits the programming current because mP supplies the elevated programming current. Next, the control voltage on g[j] during the sense operation is a short pulse of about 1ns, as compared to about 200us during fuse programming, which will limit the degree of variation in xF or xF[j] resistance. Lastly, in the case where xF[j] is already programmed, the post-program resistance will further reduce the current through xF.

[Para 27] The voltage at node F is equal to about 0.5*Vdd for an unprogrammed fuse and to about [b/(1+b)]*Vdd for a programmed fuse, where "b" is the post-fuse program to pre-fuse program resistance ratio. The distribution tail of a low-voltage post-program resistance value is expected to achieve b=10 (i.e., most post-fuse program resistances are expected to be more than about 1500 Ω).

[Para 28] Node F is coupled to the positive input Vp of DiffAmp D while the negative input Vm is a reference voltage (0.67*Vdd) established with a circuit network of three identical resistors R1, R0a, R0b and gating transistor mNR. The gating transistor mNR emulates the voltage drop through the gating transistor mN[j] when an intact fuse is sensed. As such, transistor mNR is sized to have the same current density (hence voltage drop) of transistor mN[j]. Again, the control voltage on gate gR of transistor mNR during the sense operation is a short pulse of about 1ns, which allows the duty cycle in the reference fuse chain to be low, as described in the discussion above regarding fuse xF and fuse xF[j].

[Para 29] The differential input voltage to DiffAmp D is 0.167*Vdd for an intact fuse and [(b-2)/3]*Vdd for a programmed fuse with post-programming resistance ratio "b." A post-programming resistance ratio as low as b=2.5 will produce as strong a signal response as the intact fuse.

[Para 30] Additionally, the DiffAmp output can be captured into a register with a strobe signal every time a rising edge occurs for the sense signal. The select signals are different for each successive sense signal until all fuses have been sampled, and their states stored in registers.

[Para 31] Referring to Fig. 3 again, the voltage at node Vp is determined by a voltage divider consisting of an unprogrammed fuse xF and a selected fuse xF[j] that can be either programmed or unprogrammed. Similarly, the voltage at node Vm is determined by a voltage divider consisting of resistors R1, R0a, and R0b.

[Para 32] In a second embodiment of the present invention, the fuse resistances are characterized both pre-fuse programming and post-fuse programming. The characterization feature is realized by using digital control bits with multiple settings to vary the voltages at node Vm, such that incremental changes in fuse resistances may be obtained.

[Para 33] As shown in Fig. 4, a digital control bit RU turns on transitor mRU, a large device with low resistance, such that fuse xF is now in parallel with a second unprogrammed fuse xRU. In this configuration, digital control bit RU causes an increase in the voltage at node Vp such that it is equal to the voltage on Vm if the selected fuse xF[j] is not programmed. This step by itself reduces the differential signal to zero in the case where xF[j] is unprogrammed, however, it also allows incremental adjustment of the voltage on node Vm to characterize resistance. Since the resistance of the series combination of R0a and R0b (collectively called "R0") is twice that of R1, the voltage on Vm is 0.67*Vdd. With RU=1, an ideal (i.e., no resistance anomalies) unprogrammed fuse also causes the voltage on Vp to be approximately 0.67*Vdd, so that the "threshold resistance" of fuse xF[j] approaches the ideal fuse resistance, RidealFuse.

[Para 34] Referring to Fig. 5, a voltage reference circuit establishing the voltage on Vm, including new digital control bits ML[1:0] and MR[1:0] is shown. When all ML and MR bits are zero, the voltage on Vm is derived from the voltage divider comprising resistors R1, R0a and R0b and transistor mNR.

However, when ML[1:0]=01, resistor RML0 is in parallel with R0, and Vm is reduced a small amount. The threshold of resistance on fuse xF[j] from Fig.4 is now less than RidealFuse; when ML[0:1]= 10 and 11, the voltage on Vm decreases further so that the threshold of resistance of xF[j] takes on smaller discrete values. All fuses could be sampled with different ML settings, and discrete points on the unprogrammed resistance distribution can be found for RFuse < RidealFuse.

[Para 35] Similarly, control bits MR[1:0] can be exercised to force Vm slightly higher (raising the threshold resistance above RidealFuse), so that discrete points of the unprogrammed resistance distribution can be found for RFuse > RidealFuse. In addition, if RU=0, the threshold returns to RFuse = 2*RidealFuse in the absence of any non-zero value on ML or MR pins. The unprogrammed resistances will never approach 2*RidealFuse, but post-programming resistances will generally exceed this value, which allows the post-programming resistance distribution to be characterized. Leaving ML[1:0]=00 and counting through the non-zero value on MR[1:0], the voltage on node Vm is raised further, achieving higher threshold resistance and allowing the post-programming resistance distribution to be characterized at discreet points. Toggling both ML[1:0] and MR[1:0] allows even more granularity in the distribution to be characterized, although ML pins can not increase the maximum resistance threshold.

[Para 36] To conserve area, the reference voltage network is shared with a plurality of differential amplifiers. Referring to Fig. 5, the increased complexity and size of the voltage reference circuit can be compensated for by sharing it across a larger number of DiffAmps to improve area efficiency. Because of unprogrammed fuse resistance variation, it is important to consider the reference pull up fuse xF shown in Fig.3 and Fig.4. Variation in this element introduces error into the sensing scheme described herein. Accordingly, fuse xF should be implemented as a combination of multiple fuses as shown in Fig.6 to compensate for the potential variation in resistance values for individual fuses.

[Para 37] Figs. 7A and 7B show an exemplar schematic of the additional logic required for fuse selection and a timing diagram of the associated logic transitions, respectively. The fuse programming and sensing element 20 is a block diagram representation of the fuse programming and sensing circuitry depicted in Fig. 3. Referring to Fig. 7A, one of the pins D[15:0] is brought high to select which fuse will be read. Then clock signal, Clk is brought high to initiate the read operation. One of the AND2 gates 30 which receives both Clk and a D[j] signal that is a "1" will provide a "1" output on its g[j] output. This will turn on transistor mN[j] shown in Fig.3 so that node F in Fig.3 is pulled down if the fuse is intact, or node F will remain high if the fuse is programmed. The clock signal also turns on transistor mNR depicted in the voltage divider of Fig.3. The DiffAmp output A (shown in Fig. 7A) will go to a "0" if the fuse is intact, or a "1" if the fuse is programmed. This output A is provided to the D input of each of the latches L[15:0]. However, each latch gets a unique clock g[j], and only one of these g[j] signals is active to allow just one latch L[j] to be updated with the value on its D input. Thus only one of the outputs Q[15:0] will change during a read operation.

[Para 38] While the invention has been described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is understood that numerous other modifications and variations can be devised without departing from the scope of the invention.